Claims

[c1] A method for amplifying a signal comprising:
generating an input signal; and
amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal.

[c2] A method in accordance with Claim 1 wherein amplifying the input signal comprises chopping the input signal utilizing a first NMOS depletion mode chopping switch responsive to a first chopping signal to produce a first chopped input signal.

[c3] A method in accordance with Claim 1 wherein amplifying the input signal comprises amplifying the first chopped input signal utilizing an NMOS depletion mode amplifier stage to produce an amplified chopped output signal.

[c4] A method in accordance with Claim 1 wherein amplifying the input signal comprises chopping the amplified chopped output signal utilizing an NMOS depletion mode amplifier responsive to a level shifted first chopping signal to produce a chopper-stabilized output signal.

[c5] A method in accordance with Claim 2 further comprising generating at least one opposite node of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal, and the level shifted first chopping signal in response to a clock signal.

[c6] A buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:
an input;
an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;
a buffered field effect transistor logic (BFL) stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel;

a first output at an electrical node between said voltage drop circuit and said first channel; and

a second output at an electrical node between said voltage drop circuit and said second channel.

[c7] A circuit in accordance with Claim 6 wherein said voltage drop circuit is a resistor.

[c8] A buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:

an input;

an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;

a buffered field effect transistor logic (BFL) stage responsive to said inverted output, said BFL stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel; and a resistor electrically connected in series between said first channel and said second channel;

a first output at an electrical node between said resistor and said first channel; and

a second output at an electrical node between said resistor and said second channel, wherein said circuit is fabricated on a silicon carbide substrate.

[c9] A circuit in accordance with Claim 8 configured to operate with a negative direct current (DC) bias on each said gate with respect to each said associated channel.

[c10] An operational amplifier circuit comprising:

a first NMOS depletion mode amplification stage;

a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to said first amplification stage;

a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and

an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a voltage dropping element.

[c11] A circuit in accordance with Claim 10 wherein said first voltage dropping element comprises at least one diode-connected field effect transistor (FET).

[c12] A circuit in accordance with Claim 10 wherein said voltage dropping element is a resistor, said NMOS depletion mode BFL level shifting/inverter circuit comprises a plurality of field effect transistors (FETs) each having a gate and an associated channel.

[c13] A circuit in accordance with Claim 12 wherein said BFL level shifting/inverter circuit is configured to operate with negative direct current (DC) bias on each said gate with respect to each said associated channel.

[c14] An operational amplifier circuit comprising:
a first NMOS depletion mode amplification stage;
a first NMOS depletion mode chopping switch responsive to a first chopping signal to chop an input signal to said first amplification stage;
a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal to chop an output signal from said first amplification stage; and
and an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a resistor;
and further wherein said operational amplifier circuit is fabricated on a silicon carbide substrate.

[c15] A circuit in accordance with Claim 14 wherein said first chopping switch and said second chopping switch each comprise NMOS field effect transistor (FET) switches having a channel and a gate, and said NMOS field effect transistors have threshold voltages negative with respect to their respective channels.

[c16] A circuit in accordance with Claim 14 further comprising a clock generator configured to produce said clock signal.

[c17] An operational amplifier circuit comprising:
a first NMOS depletion mode amplification stage having differential inputs and outputs;
a first NMOS depletion mode chopping switch responsive to a first chopping signal

and a second chopping signal to chop a differential input signal to said first amplification stage;

a second NMOS depletion mode chopping switch responsive to a level-shifted first chopping signal and a level shifted second chopping signal to chop an output signal from said first amplification stage;

a first NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to a clock signal to generate said first chopping signal and said level shifted first chopping signal across a first resistor;

a second NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit responsive to said clock signal to generate said second chopping signal and said level shifted second chopping signal across a second resistor; and

a clock generator circuit configured to generate said clock signal.

[c18] A circuit in accordance with Claim 17 fabricated on a silicon carbide substrate.

[c19] A circuit in accordance with Claim 17 further comprising at least one additional stage of amplification responsive to said chopped output signal from said first amplification stage.

[c20] A circuit in accordance with Claim 19 further comprising a sensor, wherein said first amplification stage is responsive to an output signal of said sensor chopped by said first NMOS depletion mode chopping switch.

[c21] A circuit in accordance with Claim 20 wherein said circuit and sensor are operated at a temperature in excess of 300 degrees Celsius.

[c22]

A method for amplifying a signal comprising:

generating an input signal;

amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier to produce an amplified output signal;

amplifying the input signal by chopping the input signal utilizing a first NMOS depletion mode chopping switch that is responsive to a first chopping signal to produce a first chopped input signal; and

amplifying the first chopped input signal utilizing an NMOS depletion mode

amplifier stage to produce an amplified chopped output signal.

[c23] A method in accordance with Claim 22 wherein amplifying the input signal utilizing a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier, comprises chopping the amplified chopped output signal utilizing an NMOS depletion mode amplifier responsive to a level shifted first chopping signal to produce a chopper-stabilized output signal.

[c24] A method in accordance with Claim 23 further comprising generating, a opposite nodes of a resistor of an NMOS depletion mode buffered field effect transistor logic (BFL) level shifting/inverter circuit, the first chopping signal and the level shifted first chopping signal in response to a clock signal.